APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,869	03/04/2005	Stefano Tomasin	IT 020026	5437

24737   7590   04/10/2008
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EXAMINER
TORRES, JUAN A

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
04/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/526,869	TOMASIN ET AL.
Office Action Summary	Examiner	Art Unit
	JUAN A. TORRES	2611

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>04 March 2005</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-12</u> is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-12</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>04 March 2005</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☒ All   b)☐ Some *   c)☐ None of:

        1.☒ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
     Paper No(s)/Mail Date <u>05/09/2007</u>.

4) ☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement filed 05/09/2007 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

The drawings are objected to because: the drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the rectangular boxes of figures 1-4 must be shown with a labeled representation (i.e. "encoder", "mapper", "modulator", "equalizer" etc...), or the feature(s) canceled from the claim(s). No new matter should be entered.

37 CFR 1.83 Content of drawing states "(a) The drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be

illustrated in the drawing in the form of a graphical drawing symbol or a labeled

representation (e.g., a labeled rectangular box).

" Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in

reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next

Office action. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper language and format for an abstract of the
disclosure.

The abstract should be in narrative form and generally limited to a single
paragraph on a separate sheet within the range of 50 to 150 words. It is important that
the abstract not exceed 150 words in length since the space provided for the abstract
on the computer tape used by the printer is limited. The form and legal phraseology
often used in patent claims, such as "means" and "said," should be avoided. The
abstract should describe the disclosure sufficiently to assist readers in deciding whether
there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because:

a) Exceed 150 words in length

b) Uses he form and legal phraseology often used in patent claims, such as

"said,"

Correction is required. See MPEP § 608.01(b).

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR
        DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A
        COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
        (1) Field of the Invention.
        (2) Description of Related Art including information disclosed under 37
        CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A
        "Sequence Listing" is required on paper if the application discloses a

nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if
the required "Sequence Listing" is not submitted as an electronic
document on compact disc).

Content of Specification

(a)   Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of
        the invention should be placed at the top of the first page of the
        specification unless the title is provided in an application data sheet. The
        title of the invention should be brief but technically accurate and
        descriptive, preferably from two to seven words may not contain more
        than 500 characters.

(b)   Cross-References to Related Applications: See 37 CFR 1.78 and MPEP
        § 201.11.

(c)   Statement Regarding Federally Sponsored Research and Development:
        See MPEP § 310.

(d)   The Names Of The Parties To A Joint Research Agreement: See 37 CFR
        1.71(g).

(e)   Incorporation-By-Reference Of Material Submitted On a Compact Disc:
        The specification is required to include an incorporation-by-reference of
        electronic documents that are to become part of the permanent United
        States Patent and Trademark Office records in the file of a patent
        application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer
        program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)),
        and tables having more than 50 pages of text were permitted as electronic
        documents on compact discs beginning on September 8, 2000.

(f)   Background of the Invention: See MPEP § 608.01(c). The specification
        should set forth the Background of the Invention in two parts:

        (1)   Field of the Invention: A statement of the field of art to which the
                invention pertains. This statement may include a paraphrasing of
                the applicable U.S. patent classification definitions of the subject
                matter of the claimed invention. This item may also be titled
                "Technical Field."

        (2)   Description of the Related Art including information disclosed under
                37 CFR 1.97 and 37 CFR 1.98: A description of the related art
                known to the applicant and including, if applicable, references to
                specific related art and problems involved in the prior art which are

solved by the applicant's invention. This item may also be titled
"Background Art."

(g)   Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary
        or general statement of the invention as set forth in 37 CFR 1.73. The
        summary is separate and distinct from the abstract and is directed toward
        the invention rather than the disclosure as a whole. The summary may
        point out the advantages of the invention or how it solves problems
        previously existent in the prior art (and preferably indicated in the
        Background of the Invention). In chemical cases it should point out in
        general terms the utility of the invention. If possible, the nature and gist of
        the invention or the inventive concept should be set forth. Objects of the
        invention should be treated briefly and only to the extent that they
        contribute to an understanding of the invention.

(h)   Brief Description of the Several Views of the Drawing(s): See MPEP §
        608.01(f). A reference to and brief description of the drawing(s) as set
        forth in 37 CFR 1.74.

(i)   Detailed Description of the Invention: See MPEP § 608.01(g). A
        description of the preferred embodiment(s) of the invention as required in
        37 CFR 1.71. The description should be as short and specific as is
        necessary to describe the invention adequately and accurately. Where
        elements or groups of elements, compounds, and processes, which are
        conventional and generally widely known in the field of the invention
        described and their exact nature or type is not necessary for an
        understanding and use of the invention by a person skilled in the art, they
        should not be described in detail. However, where particularly
        complicated subject matter is involved or where the elements,
        compounds, or processes may not be commonly or widely known in the
        field, the specification should refer to another patent or readily available
        publication which adequately describes the subject matter.

(j)   Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or
        claims must commence on separate sheet or electronic page (37 CFR
        1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each
        element or step of the claim should be separated by a line indentation.
        There may be plural indentations to further segregate subcombinations or
        related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(k)   Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the
        disclosure as a whole in a single paragraph of 150 words or less
        commencing on a separate sheet following the claims. In an international
        application which has entered the national stage (37 CFR 1.491(b)), the
        applicant need not submit an abstract commencing on a separate sheet if

an abstract was published with the international application under PCT
Article 21. The abstract that appears on the cover page of the pamphlet
published by the International Bureau (IB) of the World Intellectual
Property Organization (WIPO) is the abstract that will be used by the
USPTO. See MPEP § 1893.03(e).

(l)   Sequence Listing. See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431.
The requirement for a sequence listing applies to all sequences disclosed
in a given application, whether the sequences are claimed or not. See
MPEP § 2421.02.

35 U.S.C. 112, first paragraph, requires the specification to be written in "full,

clear, concise, and exact terms." The specification should be revised carefully in order

to comply with 35 U.S.C. 112, first paragraph.

The disclosure is objected to because of the following informalities: the recitation

"inter alia" in page 3 lines 3, 7, 18, 20, 22 and 23 is improper, because is not properly

constructed (it is not English); it is suggested to be deleted. Appropriate correction is

required.

Claim Objections

Claims 1-12 are objected to because of the following informalities:

Regarding claim 1, the recitation in line 1 of claim 1 "Filterbank-based modulation

system" is improper, because it is improperly constructed; it is suggested to be changed

to "A Filterbank-based modulation system".

Regarding claims 2-5, they are objected because they depend directly or

indirectly from claim 1 and claim 1 is objected,

Regarding claims 2-5, the recitation in line 1 of claims 2-5 "Filterbank-based

modulation system" is improper, because it is improperly constructed; it is suggested to

be changed to "The Filterbank-based modulation system".

Regarding claim 5, the recitation in line 1 of claim 5 "to claim 3, said"" is improper, because it is improperly constructed (see claims 2-4); it is suggested to be changed to "to claim 3, wherein said".

Regarding claims 6-7, the recitation in line 1 of claims 6-7 "Sender for" is improper, because it is improperly constructed; it is suggested to be changed to "A Transmitter for".

Regarding claims 1-12, the recitation in claims 1-12 "sender" is improper, because it is improperly constructed, in the art the appropriate word is transmitter to send and receiver to receive; it is suggested to be changed to "transmitter".

Regarding claims 1-12, the recitation in claims 1-12 "sending" is improper, because it is improperly constructed, in the art the appropriate word is transmitter to send and receiver to receive; it is suggested to be changed to "transmitting".

Regarding claims 8 and 11, the recitation in line 1 of claims 8 and 11 "Processor" is improper, because it is improperly constructed; it is suggested to be changed to "A processor".

Regarding claims 9 and 10, the recitation in line 1 of claims 9 and 10 "Receiver" is improper, because it is improperly constructed; it is suggested to be changed to "A receivert".

Regarding claim 12, the recitation in line 1 of claim 12 "Method" is improper, because it is improperly constructed; it is suggested to be changed to "A method".

Regarding claims 1-12, the recitation "fourier" is improper, because it is improperly constructed (Fourier is a surname); it is suggested to be changed to "Fourier".

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 8 and 11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 8 and 11 claim a "Processor program product to be run via a sender-processor" and the program is not claimed as embodied in computer-readable media, and programs not claimed as embodied in computer-readable media are descriptive material per se and are not statutory because they are not capable of causing functional change in the computer (see MPEP 2106.01)..

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Cheong ("Precoder for DMT with insufficient cyclic prefix", ICC 1998, 1998 IEEE International Conference on Communications, Publication Date: 7-11 Jun 1998, Volume: 1, On page(s): 339-343 vol.1).

Regarding claims 1 and 12, Cheong discloses a sender with a sender-processor for processing data and sending processed data to a receiver and via said receiver with a receiver-processor for receiving and processing said processed data, which method comprises the steps of performing inverse fast Fourier transformations and of filtering signals in said sender and of performing fast Fourier transformations in said receiver, said method comprising the steps of coding signals and of further filtering signals in at least one feedback loop in said sender, which coding is performed before said inverse fast Fourier transformations, and of decoding signals in said receiver, which decoding is performed after said fast Fourier transformation (section 3 figure 2).

Regarding claim 2, Cheong discloses claim 1, Cheong also discloses a splitting-module for splitting said data into signal streams and a combining-module for combining signal streams into said processed data, with said inverse-fast-Fourier-transformating-module and said filtering-module and said coding-module with said further-filtering-module in at least one feedback loop being situated between said splitting-module and said combining-module, and with said receiver-processor comprising a splitting-module for splitting said processed data into signal streams and a combining-module for combining signal streams into further processed data, with said fast-Fourier-

transformating-module and said decoding-module being situated between said splitting-module and said combining-module (section 3 figure 2, the signal enter in serial form, the Hermitian convert the signal to parallel, all the processing of the pre-coding is done in parallel for all the subcarriers, the P/S is the combiner that convert the signals back to serial, in the receiver the S/P convent the serial signals to parallel and the strip Hermitian convert to serial again).

Regarding claim 3, Cheong discloses claim 2, Cheong also discloses a sub-coding-module per signal stream, with said filtering-module comprising a sub-filtering-module per signal stream, with said further-filtering-module comprising a sub-further-filtering-module per signal stream, and with said decoding-module comprising a sub-decoding-module per signal stream (section 3 figure 2, all the processing of the pre-coding is done in the parallel in a subcarriers basis, the P/S is the combiner that convert the signals back to serial).

Regarding claim 4, Cheong discloses claim 3, Cheong also discloses sub-further-filtering-modules receive input signals from outputs of said inverse-fast-Fourier-transformating-module and supply output signals via a fast-Fourier-transformating-module to inputs of said sub-coding-modules via adding/subtracting-modules (section 3 figure 2, all the processing of the pre-coding is done in the parallel in a subcarriers basis, the P/S is the combiner that convert the signals back to serial).

Regarding claim 5, Cheong discloses claim 3, Cheong also discloses sub-further-filtering-modules receive input signals from outputs of said sub-coding-modules and supply output signal to inputs of said sub-coding-modules via adding/subtracting-

modules (section 3 figure 2, all the processing of the pre-coding is done in the parallel in a subcarriers basis, the P/S is the combiner that convert the signals back to serial).

Regarding claims 6, 7 and 8, Cheong discloses a sender-processor for processing data and sending processed data to a receiver and comprising said receiver with a receiver-processor for receiving and processing said processed data, which sender-processor comprises an inverse-fast-Fourier-transformating-module and a filtering-module and which receiver-processor comprises a fast-Fourier-transformating-module, said sender-processor comprising a coding-module with a further-filtering-module in at least one feedback loop, which coding-module is situated before said inverse-fast-Fourier-transformating-module (section 3 figure 2).

Regarding claims 9, 10 and 11, Cheong discloses a sender with a sender-processor for processing data and sending processed data to said receiver and comprising said receiver with a receiver-processor for receiving and processing said processed data, which sender-processor comprises an inverse-fast-Fourier-transformating-module and a filtering-module and which receiver-processor comprises a fast-Fourier-transformating-module, said receiver-processor comprising a decoding-module situated after said fast-Fourier-transformating-module (section 3 figure 2 transmitter side of figure 2).

Claims 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Benvenuto ("Receiver architectures for FMT broadband wireless systems" Vehicular Technology Conference, 2001. VTC 2001 Spring. IEEE VTS 53rd Volume 1, 6-9 May 2001 Page(s):643 - 647 vol.1)

Regarding claims 9, 10 and 11, Benvenuto discloses a sender with a sender-

processor for processing data and sending processed data to said receiver and

comprising said receiver with a receiver-processor for receiving and processing said

processed data, which sender-processor comprises an inverse-fast-Fourier-

transformating-module and a filtering-module and which receiver-processor comprises a

fast-Fourier-transformating-module, said receiver-processor comprising a decoding-

module situated after said fast-Fourier-transformating-module (sections 1-4 figures 1-4).

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Nedic

(US 20030063680 A1).

Regarding claims 1 and 12, Nedic discloses a sender with a sender-processor for

processing data and sending processed data to a receiver and via said receiver with a

receiver-processor for receiving and processing said processed data, which method

comprises the steps of performing inverse fast Fourier transformations and of filtering

signals in said sender and of performing fast Fourier transformations in said receiver,

said method comprising the steps of coding signals and of further filtering signals in at

least one feedback loop in said sender, which coding is performed before said inverse

fast Fourier transformations, and of decoding signals in said receiver, which decoding is

performed after said fast Fourier transformation (figures 2 and 5 paragraphs [0038] and

[0057]).

Regarding claim 2, Nedic discloses claim 1, Nedic also discloses a splitting-

module for splitting said data into signal streams and a combining-module for combining

signal streams into said processed data, with said inverse-fast-Fourier-transformating-

module and said filtering-module and said coding-module with said further-filtering-module in at least one feedback loop being situated between said splitting-module and said combining-module, and with said receiver-processor comprising a splitting-module for splitting said processed data into signal streams and a combining-module for combining signal streams into further processed data, with said fast-Fourier-transformating-module and said decoding-module being situated between said splitting-module and said combining-module (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claim 3, Nedic discloses claim 2, Nedic also discloses a sub-coding-module per signal stream, with said filtering-module comprising a sub-filtering-module per signal stream, with said further-filtering-module comprising a sub-further-filtering-module per signal stream, and with said decoding-module comprising a sub-decoding-module per signal stream (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claim 4, Nedic discloses claim 3, Nedic also discloses sub-further-filtering-modules receive input signals from outputs of said inverse-fast-Fourier-transformating-module and supply output signals via a fast-Fourier-transformating-module to inputs of said sub-coding-modules via adding/subtracting-modules (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claim 5, Nedic discloses claim 3, Nedic also discloses sub-further-filtering-modules receive input signals from outputs of said sub-coding-modules and supply output signal to inputs of said sub-coding-modules via adding/subtracting-modules (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claims 6, 7 and 8, Nedic discloses a sender-processor for processing data and sending processed data to a receiver and comprising said receiver with a receiver-processor for receiving and processing said processed data, which sender-processor comprises an inverse-fast-Fourier-transformating-module and a filtering-module and which receiver-processor comprises a fast-Fourier-transformating-module, said sender-processor comprising a coding-module with a further-filtering-module in at least one feedback loop, which coding-module is situated before said inverse-fast-Fourier-transformating-module (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claims 9, 10 and 11, Nedic discloses a sender with a sender-processor for processing data and sending processed data to said receiver and comprising said receiver with a receiver-processor for receiving and processing said processed data, which sender-processor comprises an inverse-fast-Fourier-transformating-module and a filtering-module and which receiver-processor comprises a fast-Fourier-transformating-module, said receiver-processor comprising a decoding-module situated after said fast-Fourier-transformating-module (figures 2 and 5 paragraphs [0038] and [0057]).

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Cherubini (US 6741551 B1).

Regarding claims 1 and 12, Cherubini discloses a sender with a sender-processor for processing data and sending processed data to a receiver and via said receiver with a receiver-processor for receiving and processing said processed data, which method comprises the steps of performing inverse fast Fourier transformations

and of filtering signals in said sender and of performing fast Fourier transformations in said receiver, said method comprising the steps of coding signals and of further filtering signals in at least one feedback loop in said sender, which coding is performed before said inverse fast Fourier transformations, and of decoding signals in said receiver, which decoding is performed after said fast Fourier transformation (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claim 2, Cherubini discloses claim 1, Cherubini also discloses a splitting-module for splitting said data into signal streams and a combining-module for combining signal streams into said processed data, with said inverse-fast-Fourier-transformating-module and said filtering-module and said coding-module with said further-filtering-module in at least one feedback loop being situated between said splitting-module and said combining-module, and with said receiver-processor comprising a splitting-module for splitting said processed data into signal streams and a combining-module for combining signal streams into further processed data, with said fast-Fourier-transformating-module and said decoding-module being situated between said splitting-module and said combining-module (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claim 3, Cherubini discloses claim 2, Cherubini also discloses a sub-coding-module per signal stream, with said filtering-module comprising a sub-filtering-module per signal stream, with said further-filtering-module comprising a sub-further-filtering-module per signal stream, and with said decoding-module comprising a sub-decoding-module per signal stream (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claim 4, Cherubini discloses claim 3, Cherubini also discloses sub-further-filtering-modules receive input signals from outputs of said inverse-fast-Fourier-transformating-module and supply output signals via a fast-Fourier-transformating-module to inputs of said sub-coding-modules via adding/subtracting-modules (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claim 5, Cherubini discloses claim 3, Cherubini also discloses sub-further-filtering-modules receive input signals from outputs of said sub-coding-modules and supply output signal to inputs of said sub-coding-modules via adding/subtracting-modules (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claims 6, 7 and 8, Cherubini discloses a sender-processor for processing data and sending processed data to a receiver and comprising said receiver with a receiver-processor for receiving and processing said processed data, which sender-processor comprises an inverse-fast-Fourier-transformating-module and a filtering-module and which receiver-processor comprises a fast-Fourier-transformating-module, said sender-processor comprising a coding-module with a further-filtering-module in at least one feedback loop, which coding-module is situated before said inverse-fast-Fourier-transformating-module (figures 2 and 5 paragraphs [0038] and [0057]).

Regarding claims 9, 10 and 11, Cherubini discloses a sender with a sender-processor for processing data and sending processed data to said receiver and comprising said receiver with a receiver-processor for receiving and processing said processed data, which sender-processor comprises an inverse-fast-Fourier-

transformating-module and a filtering-module and which receiver-processor comprises a

fast-Fourier-transformating-module, said receiver-processor comprising a decoding-

module situated after said fast-Fourier-transformating-module (figures 2 and 5

paragraphs [0038] and [0057]).

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ginis

(US 7158563 B2).

Regarding claims 1 and 12, Cherubini discloses a sender with a sender-

processor for processing data and sending processed data to a receiver and via said

receiver with a receiver-processor for receiving and processing said processed data,

which method comprises the steps of performing inverse fast Fourier transformations

and of filtering signals in said sender and of performing fast Fourier transformations in

said receiver, said method comprising the steps of coding signals and of further filtering

signals in at least one feedback loop in said sender, which coding is performed before

said inverse fast Fourier transformations, and of decoding signals in said receiver,

which decoding is performed after said fast Fourier transformation (figures 13 and 14 for

only one transmitter, column 21 lines 51-59).

Regarding claim 2, Cherubini discloses claim 1, Cherubini also discloses a

splitting-module for splitting said data into signal streams and a combining-module for

combining signal streams into said processed data, with said inverse-fast-Fourier-

transformating-module and said filtering-module and said coding-module with said

further-filtering-module in at least one feedback loop being situated between said

splitting-module and said combining-module, and with said receiver-processor

comprising a splitting-module for splitting said processed data into signal streams and a

combining-module for combining signal streams into further processed data, with said

fast-Fourier-transformating-module and said decoding-module being situated between

said splitting-module and said combining-module (figures 13 and 14 for only one

transmitter, column 21 lines 51-59).

Regarding claim 3, Cherubini discloses claim 2, Cherubini also discloses a sub-

coding-module per signal stream, with said filtering-module comprising a sub-filtering-

module per signal stream, with said further-filtering-module comprising a sub-further-

filtering-module per signal stream, and with said decoding-module comprising a sub-

decoding-module per signal stream (figures 13 and 14 for only one transmitter, column

21 lines 51-59).

Regarding claim 4, Cherubini discloses claim 3, Cherubini also discloses sub-

further-filtering-modules receive input signals from outputs of said inverse-fast-Fourier-

transformating-module and supply output signals via a fast-Fourier-transformating-

module to inputs of said sub-coding-modules via adding/subtracting-modules (figures 13

and 14 for only one transmitter, column 21 lines 51-59).

Regarding claim 5, Cherubini discloses claim 3, Cherubini also discloses sub-

further-filtering-modules receive input signals from outputs of said sub-coding-modules

and supply output signal to inputs of said sub-coding-modules via adding/subtracting-

modules (figures 13 and 14 for only one transmitter, column 21 lines 51-59).

Regarding claims 6, 7 and 8, Cherubini discloses a sender-processor for

processing data and sending processed data to a receiver and comprising said receiver

with a receiver-processor for receiving and processing said processed data, which sender-processor comprises an inverse-fast-Fourier-transformating-module and a filtering-module and which receiver-processor comprises a fast-Fourier-transformating-module, said sender-processor comprising a coding-module with a further-filtering-module in at least one feedback loop, which coding-module is situated before said inverse-fast-Fourier-transformating-module (figures 13 and 14 for only one transmitter, column 21 lines 51-59).

Regarding claims 9, 10 and 11, Cherubini discloses a sender with a sender-processor for processing data and sending processed data to said receiver and comprising said receiver with a receiver-processor for receiving and processing said processed data, which sender-processor comprises an inverse-fast-Fourier-transformating-module and a filtering-module and which receiver-processor comprises a fast-Fourier-transformating-module, said receiver-processor comprising a decoding-module situated after said fast-Fourier-transformating-module (figures 13 and 14 for only one transmitter, column 21 lines 51-59).

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Betts (US 6715124 B1).

Regarding claims 1 and 12, Cherubini discloses a sender with a sender-processor for processing data and sending processed data to a receiver and via said receiver with a receiver-processor for receiving and processing said processed data, which method comprises the steps of performing inverse fast Fourier transformations and of filtering signals in said sender and of performing fast Fourier transformations in said receiver, said method comprising the steps of coding signals and of further filtering signals in at least one feedback loop in said sender, which coding is performed before said inverse fast Fourier transformations, and of decoding signals in said receiver, which decoding is performed after said fast Fourier transformation (abstract, figures 3 and 5 precoder block 316 the trellis encoder and the precoder is tone basis column 7 line 65 to column 8 line 33).

Regarding claim 2, Cherubini discloses claim 1, Cherubini also discloses a splitting-module for splitting said data into signal streams and a combining-module for combining signal streams into said processed data, with said inverse-fast-Fourier-transformating-module and said filtering-module and said coding-module with said further-filtering-module in at least one feedback loop being situated between said splitting-module and said combining-module, and with said receiver-processor comprising a splitting-module for splitting said processed data into signal streams and a combining-module for combining signal streams into further processed data, with said fast-Fourier-transformating-module and said decoding-module being situated between

said splitting-module and said combining-module (abstract, figures 3 and 5 precoder

block 316 the trellis encoder and the precoder is tone basis column 7 line 65 to column

8 line 33).

Regarding claim 3, Cherubini discloses claim 2, Cherubini also discloses a sub-

coding-module per signal stream, with said filtering-module comprising a sub-filtering-

module per signal stream, with said further-filtering-module comprising a sub-further-

filtering-module per signal stream, and with said decoding-module comprising a sub-

decoding-module per signal stream (abstract, figures 3 and 5 precoder block 316 the

trellis encoder and the precoder is tone basis column 7 line 65 to column 8 line 33).

Regarding claim 4, Cherubini discloses claim 3, Cherubini also discloses sub-

further-filtering-modules receive input signals from outputs of said inverse-fast-Fourier-

transformating-module and supply output signals via a fast-Fourier-transformating-

module to inputs of said sub-coding-modules via adding/subtracting-modules (abstract,

figures 3 and 5 precoder block 316 the trellis encoder and the precoder is tone basis

column 7 line 65 to column 8 line 33).

Regarding claim 5, Cherubini discloses claim 3, Cherubini also discloses sub-

further-filtering-modules receive input signals from outputs of said sub-coding-modules

and supply output signal to inputs of said sub-coding-modules via adding/subtracting-

modules (abstract, figures 3 and 5 precoder block 316 the trellis encoder and the

precoder is tone basis column 7 line 65 to column 8 line 33).

Regarding claims 6, 7 and 8, Cherubini discloses a sender-processor for

processing data and sending processed data to a receiver and comprising said receiver

with a receiver-processor for receiving and processing said processed data, which

sender-processor comprises an inverse-fast-Fourier-transformating-module and a

filtering-module and which receiver-processor comprises a fast-Fourier-transformating-

module, said sender-processor comprising a coding-module with a further-filtering-

module in at least one feedback loop, which coding-module is situated before said

inverse-fast-Fourier-transformating-module (abstract, figures 3 and 5 precoder block

316 the trellis encoder and the precoder is tone basis column 7 line 65 to column 8 line

33).

Regarding claims 9, 10 and 11, Cherubini discloses a sender with a sender-

processor for processing data and sending processed data to said receiver and

comprising said receiver with a receiver-processor for receiving and processing said

processed data, which sender-processor comprises an inverse-fast-Fourier-

transformating-module and a filtering-module and which receiver-processor comprises a

fast-Fourier-transformating-module, said receiver-processor comprising a decoding-

module situated after said fast-Fourier-transformating-module (abstract, figures 3 and 5

precoder block 316 the trellis encoder and the precoder is tone basis column 7 line 65

to column 8 line 33).

The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure:

a) Scaglione ("Redundant filterbank precoders and equalizers. I. Unification and

optimal designs", IEEE Transactions on Signal Processing, Volume 47, Issue 7, July

1999 Page(s):1988 – 2006).

b) Scaglione ("Redundant filterbank precoders and equalizers. II. Blind channel estimation, synchronization, and direct equalization", Transactions on Signal Processing, IEEE Volume 47, Issue 7, July 1999 Page(s):2007 – 2022).

c) Scaglione ("Filterbank transceivers optimizing information rate in block transmissions over dispersive channels" IEEE Transactions on Information Theory, Volume 45, Issue 3, April 1999 Page(s):1019 – 1032).

d) Cacopardi ("Combined OFDM-CDMA configuration for multimedia wireless applications", IEEE Transactions on Consumer Electronics, Publication Date: Nov 1996, Volume: 42, Issue: 4, On page(s): 865-873, Meeting Date: 06/05/1996 - 06/07/1996, Location: Rosemont, IL, USA).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUAN A. TORRES whose telephone number is (571)272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Juan Alberto Torres
04/08/2008

/Juan A Torres/
Examiner, Art Unit 2611